REMARKS

Claims 1-10 are pending. Claim 3 has amended. No new matter has been added by way of this amendment. Reconsideration of the application is respectfully requested.

Claims 1 and 3-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,606,088 to *Yang* et al. in view of Pub. No.: US 2002/0122041 to Kai et al. ().and further in view of U.S. Patent No. 6,229,513 *Nakano* et al., while claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the same references, and in further view of U.S. Patent No. 6,373,476 to *Dalgliesh*. For the following reasons, these several rejection are respectfully traversed.

Set forth on page 2, paragraph 3 of the Office Action is the statement that:

> Yang differs from claim 1 in that he does not specifically teach the control signal that controls the scale module...However, referring to Fig. 5, Kai teaches a micro-processing device ([MPU] 46) adapted to output a control signal that controls the scale module ([timing pulse generation circuit] 43).

However, as set forth in claim 1 of the present invention, the scale module is provided to receive the first digital video signal and the micro–processing device is adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver *based on the first digital video signa*l.

In contrast, as taught in the *Kai* et al. publication, a video signal VB is converted from a signal processing circuit 20 to the data driver 30 (see paragraph [0044]), directly without processing through the scale module (timing pulse generation circuit 43). As shown in Fig. 1 of the *Kai* et al. publication, the video signal VB and the output pixel clock CLKD are individually transferred to the data drier 30, wherein the video signal VB is never processed through the control circuit 40.

Therefore, Applicants respectfully assert that *Kai* et al. fails to teach or suggest "the scale module provided to receive the first digital video signal," as set forth in claim 1.

Furthermore, with respect to the invention set forth in the *Kai* et al. publication, the MPU 46 is provided with a table ROM, comparing the horizontal cycle time TH and vertical cycle time TF emanating from the cycle time detecting circuit 45 with the data in the table ROM. It is provided only for determining the q and p values for generating the pixel clock CLKD (see paragraph [0064]), without any video signal being involved. That is, the *Kai* et al. publication fails to teach or suggest "the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver *based on the first digital video signal.*" Since the timing pulse generation circuit 43 and MPU 46 in the Kai et al. publication is not equivalent to the scale module 22 and MPD 23 of the present invention, Applicants respectfully assert that the rejection set forth in the Office Action based on the combined references, fails to provide an element-by-element analysis of Applicants' pending claim 1.

Although *Nakano* et al. discloses an LCD apparatus with shield cases LF1, LF2 and SHD, Applicants respectfully assert that *Nakano* et al. fails to teach, nor would it have been obvious to a person of ordinary skill in the art to use "the scale module provided to receive the first digital video signal" and "the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver based on the first digital video signal," as set forth in claim 1 of the present invention.

As stated previously, The Office Action fails to appropriately indicate each corresponding element in claim 1 of the present application. That is, neither *Yang* et al., *Kai* et al. nor *Nakano* et al. disclose all of the elements set forth in claim 1. In addition, Applicants respectfully assert that there is no motivation, teaching, nor suggestion to combine the cited

references so as to use the scale module provided to receive the first digital video signal and the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver based on the first digital video signal, as set forth in claim 1 of the present invention. In view of the foregoing, it is therefore Applicants' belief that claim 1 is allowable over the cited references, and a notice to that effect is respectfully requested.

Insofar as claims 3-10 depend from claim 1, it is Applicant's belief that these claims are also allowable.

U.S. Patent No. 6,373,476 to *Dalgleish* discloses a video signal comprising an EDID signal, however, he fails to teach or suggest the scale module and the micro-processing device as claimed in claim 1 of the present invention. Insofar as claim 2 depends from claim 1, it is Applicant's belief that claim 2 is also allowable.

Based on the foregoing remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

Dated: March 15, 2004

Respectfully submitted,

By _____

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